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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

| EXAMINER | |
|---|---|
| GEIB, BENJAMIN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/611,344 | MACY ET AL. | |
| | Examiner | Art Unit | |
| | Benjamin P. Geib | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *see continuation on next page*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Responsive to communications filed on: 06/30/2003, 10/28/2003, and 10/12/2005

## DETAILED ACTION

1. Claims 1-53 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 06/30/2003, Declaration on 10/28/2003, and Information Disclosure Statement on 10/12/2005.

### *Claim Objections*

3. Claim 31 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 30, which claim 31 depends from, already contains the limitation "wherein each of said L masks occupies a particular position in said second operand and is associated with a similarly located data element position in a resultant" and, therefore, claim 31 fails to further limit the subject matter of the claim 30.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-11, 21-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Referring to claim 1, 21 the phrase "for each control element, shuffling data from a first operand data element designated by said control element to an associated resultant data element position if its flush to zero field is not set and placing a zero into said associated resultant data element position if its flush to zero field is not set" is indefinite because it is unclear what action is to be taken when the "flush to zero" field is not set. Since the specification indicates that a zero is placed into the resultant data element position if its "flush to zero" field is set *(See paragraph 72)*, the abovementioned phrase will be interpreted as "for each control element, shuffling data from a first operand data element designated by said control element to an associated resultant data element position if its flush to zero field is not set and placing a zero into said associated resultant data element position if its flush to zero field is set" for the remainder of the examination.

7. All claims rejected by 35 U.S.C. 112, second paragraph, that have not been specifically addressed above are rejected on the basis of dependence.

### *Claim Rejections - 35 USC § 101*

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. The claimed invention is directed to non-statutory subject matter. Claim 21 refers to "machine readable medium", which is defined within the specification as including "any mechanism for storing or transmitting information in a form readable by a machine (e.g. a computer), but is not limited to, floppy disks, optical disks, ... a transmission over

the Internet, electrical, optical, acoustical or other forms of propagated signals ..." (paragraphs 34 & 35, pages 9-10)." This definition includes transmission media, which is non-statutory subject matter.

### *Claim Rejections - 35 USC § 102*

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-5, 7-10, 12-15, 18-19, 21, 29-32, 36-37, 48-49, and 51-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Rice et al., U.S. Patent No. 6,816,961 (Herein referred to as Rice).

12. Referring to claim 1, Rice has taught a method comprising:

receiving a first operand *(first source register; Fig. 5, component 504)* having a set of L data elements *(source field; Fig. 5, component 512)* and a second operand *(second source register; Fig. 7, component 508)* having a set of L control elements *(condition field; Fig. 7, component 700) (column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*; and

for each control element *(condition field)*, shuffling data from a first operand data element *(source field)* designated by said control element *(condition field)* to an associated resultant data element position *(result field; Fig. 5, component 528)* if its flush to zero field *(operation field)* is not set *(operation field = 00000; See Table I)* and placing a zero into said associated resultant data element position *(result field)* if its flush to zero field *(operation field)* is set *(operation field = 00001; See Table I) (column 6, line 62 – column 7, line 10; column 7, lines 33-67).*

13. Referring to claim 2, Rice has taught the method of claim 1 wherein each of said L control elements *(condition field)* occupies a particular position in said second operand *(second source register)* and is associated with a similarly located data element position in a resultant *(destination register) (column 6, line 62 – column 7, line 2; See Fig. 7).*

14. Referring to claim 3, Rice has taught the method of claim 2 wherein each of said L data elements *(source fields)* occupies a particular position in said first operand *(Each source field in the first source register occupies a particular position; See Fig. 7, component 512).*

15. Referring to claim 4, Rice has taught the method of claim 3 wherein said control element *(condition field)* is to designate a first operand data element *(source filed)* by a data element position number *(result field select value) (column 7, lines 49-55).*

16. Referring to claim 5, Rice has taught the method of claim 4 wherein each of said control elements *(condition fields)* is comprised of:

a flush to zero field *(operation field)*, said flush to zero field to indicate whether a data element position *(result field)* associated with this control element *(condition field)* is to be filled with a zero value *(set to low; column 7, lines 50-67; Table I)*; and

a selection field *(result field select value)*, said selection field to indicate which first operand data element *(source field)* to shuffle data from *(column 7, lines 50-55)*.

17. Referring to claim 7, Rice has taught the method of claim 2 further comprising outputting a resultant data block comprising data that was shuffled from said first operand in response to said control elements of said second operand (column 7, lines 32-42).

18. Referring to claim 8, Rice has taught the method of claim 1 wherein each of said data elements comprises a byte of data (column 6, line 62 – column 7, line 5; See Fig. 7, component 512).

19. Referring to claim 9, Rice has taught the method of claim 8 wherein each of said control elements is a byte wide (column 6, line 62 – column 7, line 5; See Fig. 7, component 700).

20. Referring to claim 10, Rice has taught the method of claim 9 wherein L is 8 and wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data (column 6, lines 19-23; See Fig. 7, components 504, 508, and 524).

21. Referring to claim 12, Rice has taught an apparatus comprising: an execution unit *(processing core; Fig. 1, component 12)* to execute a shuffle instruction *(byte swap instruction)* including a first operand *(first source register; Fig. 5, component 504)*

comprised of a set of L data elements *(source field; Fig. 5, component 512)* and a second operand *(second source register; Fig. 7, component 508)* comprised of a set of L control elements *(condition field; Fig. 7, component 700)*, said shuffle instruction to cause said execution unit to: for each individual control element *(condition field)*, determine whether its flush to zero field is set *(operation field = 00001; See Table I)*, and place a zero into an associated resultant data element position *(result field)* if true, otherwise shuffle data from a first operand data element designated by said individual control element to said associated resultant data element position *(column 6, line 62 – column 7, line 10; column 7, lines 33-67)*.

22. Referring to claim 13, given the similarities between claim 2 and claim 13 the arguments as stated for the rejection of claim 2 also apply to claim 13.

23. Referring to claim 14, given the similarities between claim 4 and claim 14 the arguments as stated for the rejection of claim 4 also apply to claim 14.

24. Referring to claim 15, given the similarities between claim 5 and claim 15 the arguments as stated for the rejection of claim 5 also apply to claim 15.

25. Referring to claim 18, given the similarities between claim 9 and claim 18 the arguments as stated for the rejection of claim 9 also apply to claim 18.

26. Referring to claim 19, given the similarities between claim 10 and claim 19 the arguments as stated for the rejection of claim 10 also apply to claim 19.

27. Referring to claim 21, Rice has taught an article comprising a machine readable medium that stores data representing a predetermined function comprising:

receiving a first operand *(first source register; Fig. 7, component 504)* having a set of L data elements *(source fields; Fig. 7, component 512)* and a second operand *(second source register; Fig. 7, component 508)* having a set of L control elements *(condition fields; Fig. 7, component 700) (column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*; and

for each control element *(condition field)*, shuffling data from a first operand data element *(source field)* designated by said control element to an associated resultant data element position *(result field; Fig. 5, component 528)* its flush to zero field *(operation field)* is not set *(operation field = 00000; See Table I)* and placing a zero into said associated resultant data element position its a flush to zero field is set *(operation field = 00001; See Table I) (column 6, line 62 – column 7, line 10; column 7, lines 33-67)*.

28. Referring to claim 29, Rice has taught the article of claim 21 wherein said data stored by said machine readable medium *(memory; column 3, lines 1-26)* represents a computer instruction, which, if executed by a machine, causes said machine to perform said predetermined function *(column 6, lines 25-53)*.

29. Referring to claim 30, given the similarities between claim 2 and claim 30 the arguments as stated for the rejection of claim 2 also apply to claim 30.

30. Referring to claim 31, given the similarities between claim 2 and claim 31 the arguments as stated for the rejection of claim 2 also apply to claim 31.

31. Referring to claim 32, given the similarities between claim 5 and claim 32 the arguments as stated for the rejection of claim 5 also apply to claim 32.

32. Referring to claim 36, given the similarities between claim 2 and claim 36 the arguments as stated for the rejection of claim 2 also apply to claim 36.

33. Referring to claim 37, given the similarities between claim 5 and claim 37 the arguments as stated for the rejection of claim 5 also apply to claim 37.

34. Referring to claim 48, Rice has taught a system comprising:

a memory to store data and instructions *(memory; Fig. 1, component 14)*;

a processor *(processing core; Fig. 1, component 12)* coupled to said memory on a bus *(See Fig. 1)*, said processor operable to perform a shuffle operation *(byte swap instruction; column 6, lines 25-54)*, said processor comprising:

a bus unit *(See Fig. 1)* to receive an instruction from said memory, said instruction to cause a data shuffle on at least one of L data elements *(source fields; Fig. 5, component 512)* from a first operand *(first source register; Fig. 5, component 504)* based on a set of L shuffle control elements *(condition fields; Fig. 7, component 700)* from a second operand *(second source register; Fig. 7, component 508)*;

an execution unit *(processing path; Fig. 2, component 56)* coupled to said bus unit, said execution unit to execute said instruction *(column 4, lines 46-61)*, said instruction to cause said execution unit to:

for each shuffle control element *(condition fields)*, shuffle data from a first operand data element *(source fields)* designated by said shuffle control element *(condition fields)* to an associated resultant data element position *(result field; Fig. 7, component 528)* if its flush to zero field

*(operation field)* is not set and place a zero into said associated resultant data element position if its flush to zero field is not set *(column 7, lines 33-67)*.

35. Referring to claim 49, given the similarities between claim 5 and claim 49 the arguments as stated for the rejection of claim 5 also apply to claim 49.

36. Referring to claim 51, Rice has taught the system of claim 48 wherein said instruction is a packed byte shuffle instruction with flush to zero capability (*column 6, lines 25-54; column 7, lines 56-67; Table I*).

37. Referring to claim 52, Rice has taught the system of claim 48 wherein each data element *(source fields; Fig. 7, component 512)* is a byte wide, each shuffle command element *(condition fields; Fig. 7, component 700)* is a byte wide, and L is 8 *(See Fig. 7)*.

38. Referring to claim 53, Rice has taught the system of claim 48 wherein said first operand *(first source register; Fig. 7, component 504)* is 64 bits long and said second operand *(second source register; Fig. 7, component 508)* is 64 bits long (See Fig. 7).

### *Claim Rejections - 35 USC § 103*

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 11, 20, and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice.

41. Referring to claim 11, Rice has taught the method of claim 9 wherein L is 8 and wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data *(column 6, lines 1-23)*.

Rice has not explicitly taught that L is 16 and wherein the first operand, second operand, and said resultant are each comprised of 128-bit wide packed data.

Q.P 12/22/05

However, the ~~Office~~ examiner takes Official Notice that 128-bit wide packed data operands are conventional and well known means of allowing an operation to be performed upon more byte sized elements at a time than a 64-bit wide packed data operand.

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the packed data operands of Rice to be 128-bit wide instead of 64-bit wide.

42. Referring to claim 20, given the similarities between claim 11 and claim 20 the arguments as stated for the rejection of claim 11 also apply to claim 20.

43. Referring to claim 22, Rice has taught the article of claim 21.

Rice has not explicitly taught that said data stored by said machine readable medium represents an integrated circuit design, which when fabricated performs said predetermined function in response to a single instruction.

However, the Office take Official Notice that a Hardware Description Language (HDL) data representation of an integrated circuit design, stored by a machine readable medium, that when fabricated performs a predetermined function in response to single instruction is a conventional and well known means to store an integrated circuit design.

Therefore, It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the data stored on a machine readable medium of Rice to be a Hardware Description Language data representation of an integrated circuit design on a machine readable medium that when fabricated performs a predetermined function in response to a single instruction.

44. Referring to claim 23, given the similarities between claim 17 and claim 23 the arguments as stated for the rejection of claim 17 also apply to claim 23.

45. Referring to claim 24, given the similarities between claim 2 and claim 24 the arguments as stated for the rejection of claim 2 also apply to claim 24.

46. Referring to claim 25, given the similarities between claim 4 and claim 25 the arguments as stated for the rejection of claim 4 also apply to claim 25

47. Referring to claim 26, given the similarities between claim 8 and claim 26 the arguments as stated for the rejection of claim 8 also apply to claim 26.

48. Referring to claim 27, given the similarities between claim 5 and claim 27 the arguments as stated for the rejection of claim 5 also apply to claim 27.

49. Claims 6, 16-17, 28, 33-35, 38, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice in view of Dulong et al., U.S. Patent Application Publication 2002/0002666 (Herein referred to as Dulong).

50. Referring to claim 6, Rice has taught the method of claim 5.

Rice has not explicitly taught that each of said control elements is further comprised of a source select field.

Dulong also taught a system for selectively storing byte fields from a source register into a destination register *(Dulong; paragraph 8)*. Dulong has further taught specifying the source for the byte field from multiple source registers using a source select field *(Dulong; condition operand; paragraphs 22-24; Fig. 2 & 3)*.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the control element of Rice to include a source select field as taught by Dulong since Dulong has taught doing so allows the selection of multiple operands based upon a condition *(Dulong; paragraph 5)*.

51. Therefore, it would have been obvious to combine Dulong with Rice to obtain the invention as specified in claim 6.

52. Referring to claim 16, given the similarities between claim 6 and claim 16 the arguments as stated for the rejection of claim 6 also apply to claim 16.

53. Referring to claim 17, Rice and Dulong have taught the apparatus of claim 16 wherein said shuffle instruction is to further cause said execution unit to generate a resultant having L data element positions that have been filled based on said set of L control elements *(Rice; column 7, lines 32-42)*.

54. Referring to claim 28, given the similarities between claim 6 and claim 28 the arguments as stated for the rejection of claim 6 also apply to claim 28.

55. Referring to claim 33, given the similarities between claim 6 and claim 33 the arguments as stated for the rejection of claim 6 also apply to claim 33.

56. Referring to claim 34, Rice and Dulong have taught the method of claim 33 wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data (column 6, lines 19-23; See Fig. 7, components 504, 508, and 524).

57. Referring to claim 35, given the similarities between claim 11 and claim 35 the arguments as stated for the rejection of claim 11 also apply to claim 35.

58. Referring to claim 38, given the similarities between claim 6 and claim 38 the arguments as stated for the rejection of claim 6 also apply to claim 38.

59. Referring to claim 50, given the similarities between claim 6 and claim 50 the arguments as stated for the rejection of claim 6 also apply to claim 50.

60. Claims 39-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice in view of Hoyle et al., U.S. Patent Application Publication 2005/0188182 (Herein referred to as Hoyle).

61. Referring to claim 39, Rice has taught an apparatus comprising:

a first memory location *(first source register; Fig. 5, component 504)* to store a plurality of source data elements *(source fields; Fig. 5, component 512)*;

a second memory location *(second source register; Fig. 7, component 508)* to store a plurality of control elements *(condition fields; Fig. 7, component 700)*, each of said control elements to correspond to a resultant data element position *(result field;*

*Fig. 7, component 528) (column 6, line 62 – column 7, line 2; See Fig. 7)*, and each of said control elements to include a flush to zero field *(operation field)* and a selection field *(result field select value) (column 7, lines 50-67)*;

control logic *(logic wires from second source register; See Fig. 7)* coupled to said second memory location *(second source register)*, said control logic in response to values of said control elements to generate a plurality of selection signals and a plurality of flush to zero signals;

a first plurality of multiplexers *(multiplexers; Fig. 7)* coupled to said first memory location *(second source register)* and said plurality of selection signals (*logic wires from second source register)*, each of said first plurality of multiplexers to shuffle a data element *(source field)* for a specific resultant data element position *(result field)* in response to a selection signal corresponding to said specific resultant data element position *(column 7, lines 2-10, 33-49)*; and

a processing component *(operand processor; Fig. 7, component 704)* coupled to said first plurality of multiplexers and to said plurality of flush to zero signals, each of said processing components associated with a specific resultant data element position *(result field)*, each of said processing components to output a zero if its flush to zero signal is active or to output a data element shuffled for that specific resultant data element position *(column 7, lines 43-67; Table I)*.

Rice has not explicitly taught that the processing components are multiplexers.

Hoyle also taught a system for intermingling/swapping bytes that uses a plurality of multiplexers to select between zero and a shuffled data element *(See Fig. 7c, paragraphs 94-96, 119)*.

It would have obvious at the time the invention was made to one of ordinary skill in the art to replace the processing component *(operand processor)* of Rice with the multiplexer of Hoyle since one of ordinary skill in the art would have recognized that doing so would allow a simpler, and possibly faster, means for selection between zero and a shuffled data element.

Therefore, it would have been obvious to combine Hoyle with Rice to obtain the invention as specified in claim 39.

62. Referring to claim 40, Rice and Hoyle have taught the apparatus of claim 39 wherein said plurality of source data elements *(source fields)* is a first packed data operand *(column 6, lines 38-41; column 6, line 62 – column 7, line 5)*.

63. Referring to claim 41, Rice and Hoyle have taught the apparatus of claim 40 where said plurality of control elements *(condition fields)* is a second packed data operand *(column 6, lines 38-41; column 6, line 62 – column 7, line 5)*.

64. Referring to claim 42, Rice and Hoyle have taught the apparatus of claim 40 wherein said first and second memory locations are a single instruction multiple data registers *(column 5, lines 58-67)*.

65. Referring to claim 43, Rice and Hoyle have taught the apparatus of claim 42 wherein:

said first packed operand is 64 bits long and each of said source data elements is a byte wide *(column 6, lines 19-22; column 6, line 62 – column 7, line 5)*; and

said second packed operand is 64 bits long and each of said control elements is a byte wide *(column 6, lines 19-22; column 6, line 62 – column 7, line 5)*.

66. Referring to claim 44, given the similarities between claim 11 and claim 44 the arguments as stated for the rejection of claim 11 also apply to claim 44.

67. Referring to claim 45, Rice has taught an apparatus comprising:

control logic *(logic wires from second source register; See Fig. 7)* to receive a set of L shuffle masks *(condition fields; Fig. 7, component 700)*, wherein each shuffle mask is associated with a unique resultant data element position *(result field; Fig. 7, component 528)*, said control logic to provide a select signal *(result field select value output)* and a flush to zero signal *(operation field output)* for each resultant data element position; and *(column 7, lines 2-10, 50-67; See Fig. 7)*

a set of L processing components *(operand processors)* coupled to said control logic, wherein each processing component is also associated with a unique resultant data element position *(result field)*, each processing component to output a zero if its associated flush to zero signal is active and to output data shuffled from a set of M data elements based on its associated select signal if its associated flush to zero signal is inactive *(column 7, lines 43-67; Table I)*.

Rice has not explicitly taught that the processing components are multiplexers.

Hoyle also taught a system for intermingling/swapping bytes that uses a plurality of multiplexers to select between zero and a shuffled data element *(See Fig. 7c, paragraphs 94-96, 119)*.

It would have obvious at the time the invention was made to one of ordinary skill in the art to replace the processing component *(operand processor)* of Rice with the multiplexer of Hoyle since one of ordinary skill in the art would have recognized that doing so would allow a simpler, and possibly faster, means for selection between zero and a shuffled data element.

Therefore, it would have been obvious to combine Hoyle with Rice to obtain the invention as specified in claim 45.

68. Referring to claim 46, Rice and Hoyle have taught the apparatus of claim 45 further comprising a register *(destination register; Fig. 7, component 524)* with L unique data element positions *(result field; Fig. 7, component 528)*, each data element position to hold an output from its associated multiplexer *(column 7, lines 33-49; See Fig. 7)*.

69. Referring to claim 47, given the similarities between claim 11 and claim 47 the arguments as stated for the rejection of claim 11 also apply to claim 47.

## ***Conclusion***

70. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

DOV POPOVICI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100